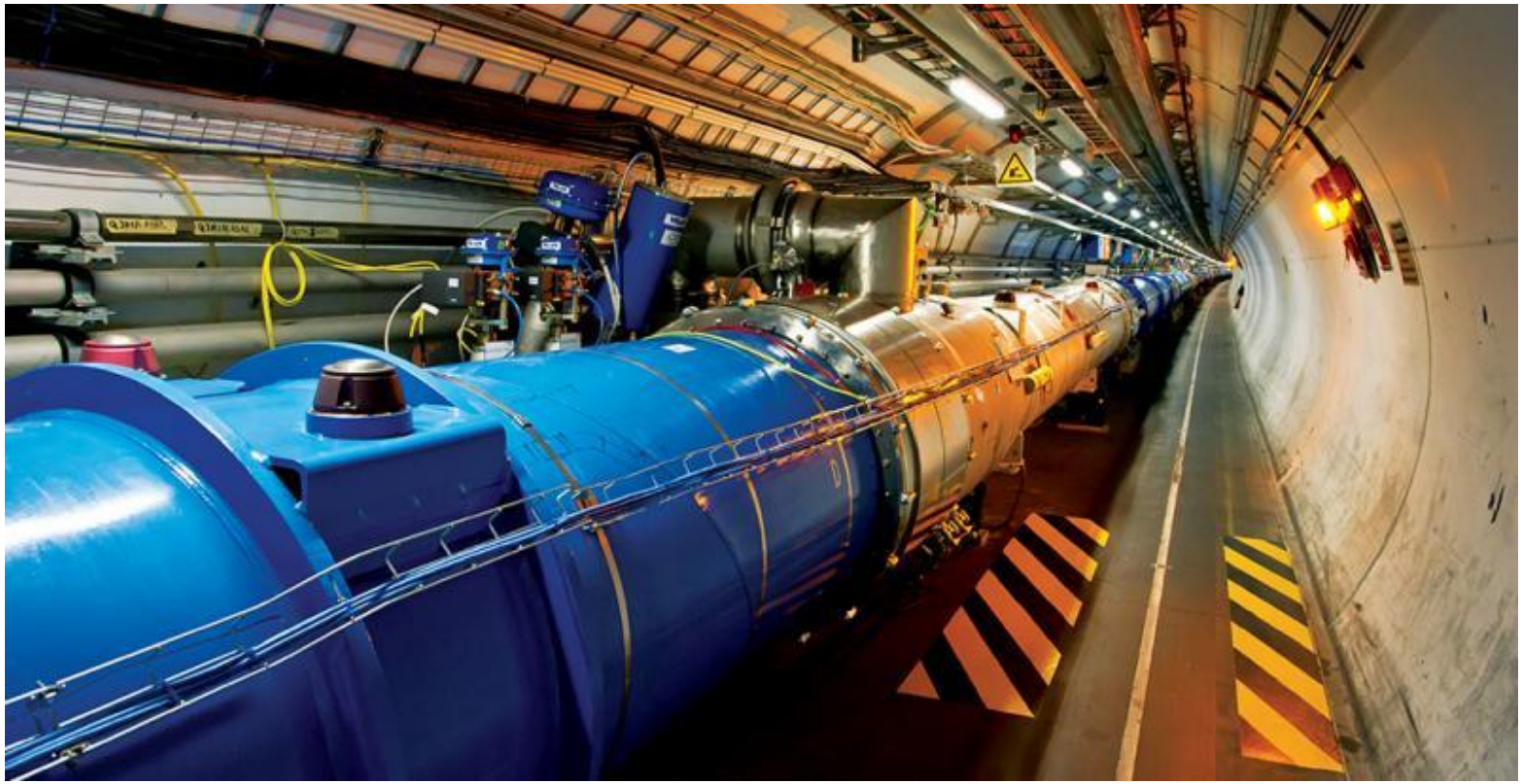


High DR ADC for LHC

Sarthak Kalani

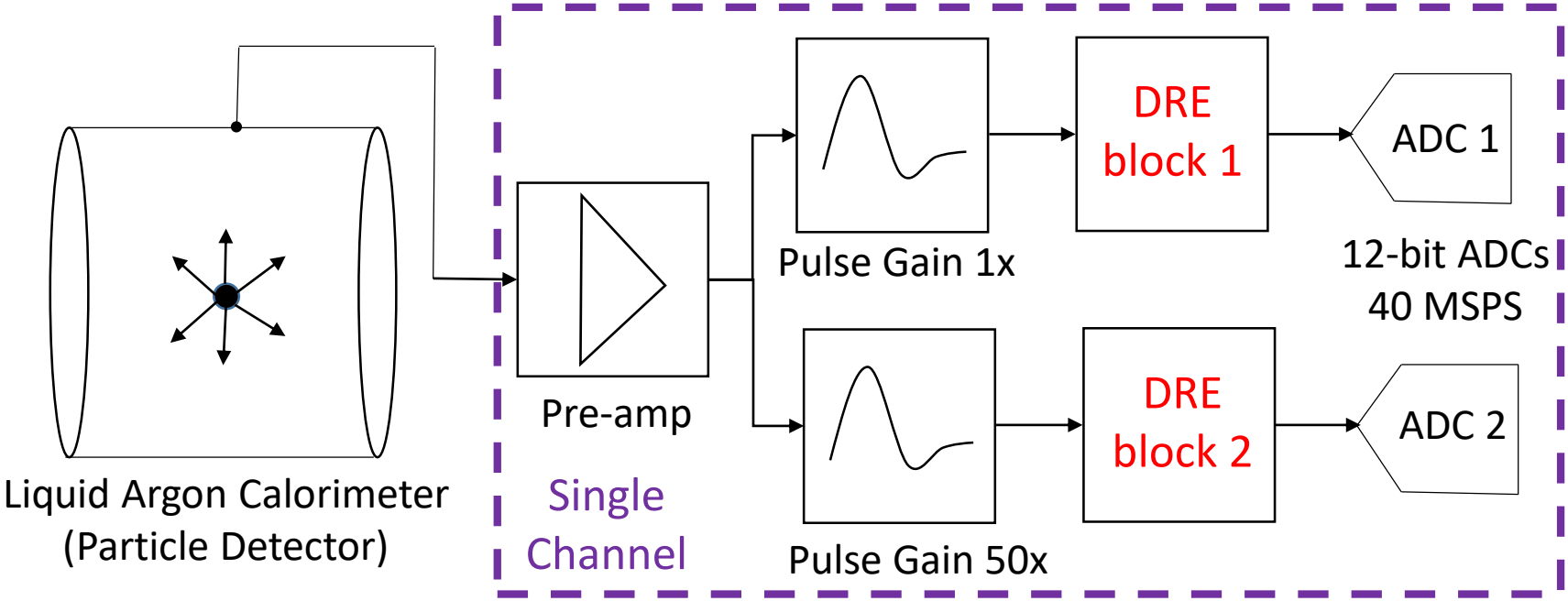
Last updated: 03/03/17

COLUMBIA UNIVERSITY
IN THE CITY OF NEW YORK

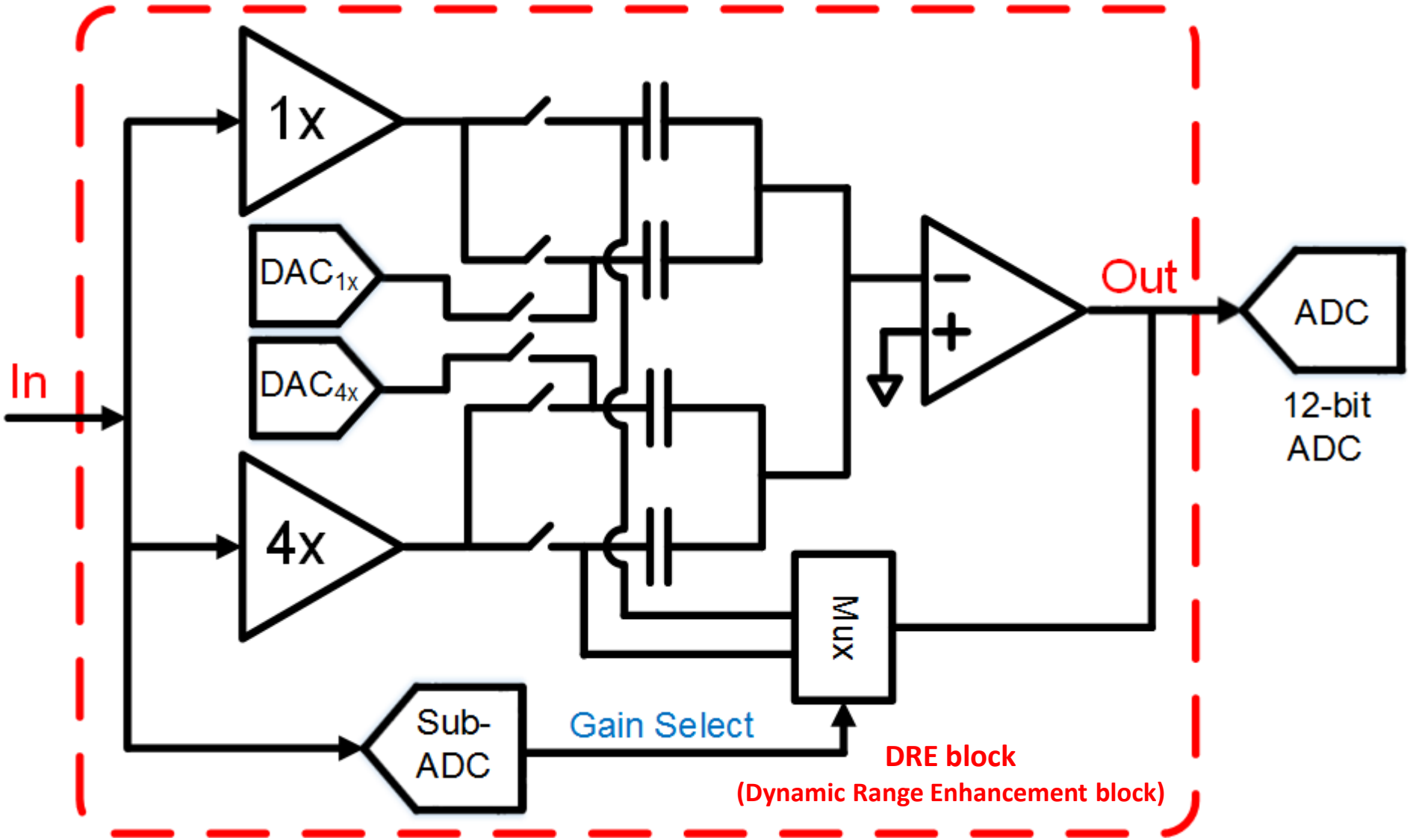
Columbia Integrated Systems Laboratory

Aim: ADC design for The LHC (Large Hadron Collider), CERN

- ADC specifications:
  - 14-bit design: To accommodate high dynamic range (16 bit)
  - 40MSps
- To design: intermediate block
  - Increase accuracy to 14 bit (or enhance the dynamic range)



Modified MultiGain (MMG) Scheme

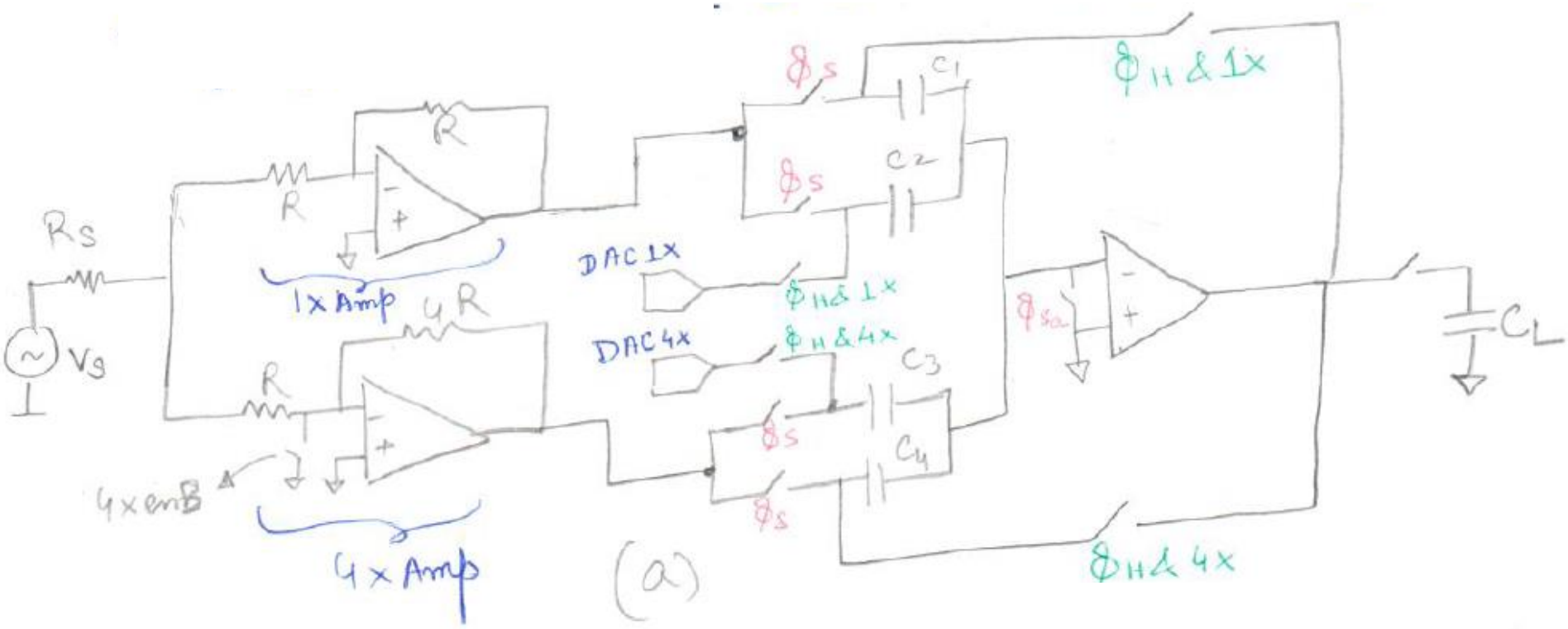


Updates from the last month

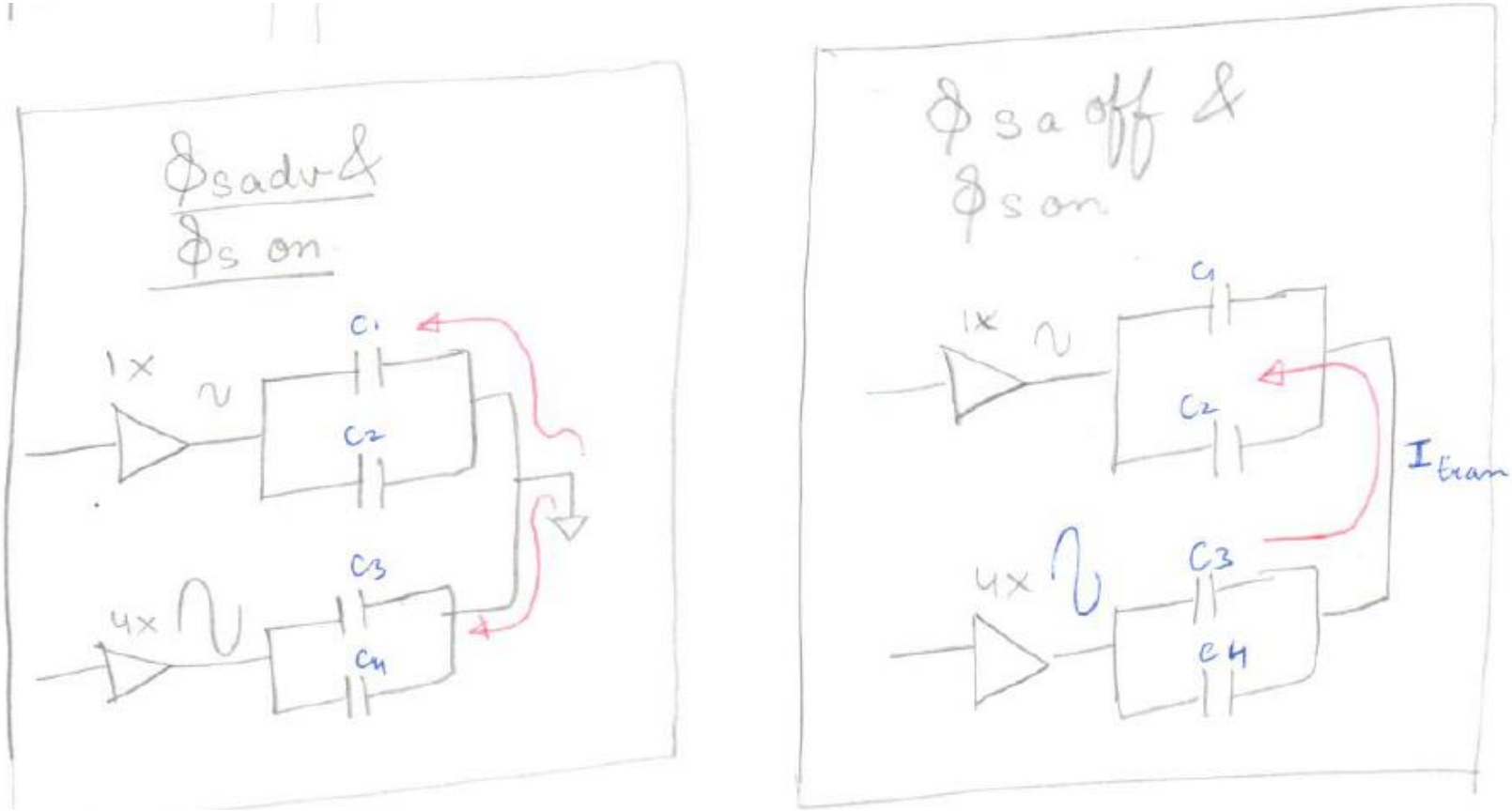
- Design moved to LVT transistors.
- Power reduction -> 35mA per Opamp (instead of 60mA per Opamp).
- Forced 4x branch select: 68dB SFDR was obtained.
- Forced 1x branch select: 34dB SFDR was obtained!!
- The problem and solution explained in next slide.
- **Later update**: Obtained better than 67dB SFDR over PT for forced 1x branch or forced 4x branch selection ($1.6V_{pp}$ Differential output for both).
- Autoselect scheme: For ideal amplifier and switch case, obtained 73dB SNDR

Reason for 34dB SFDR for 1.6V_{pp} diff input

Detailed overall diagram with switch timing

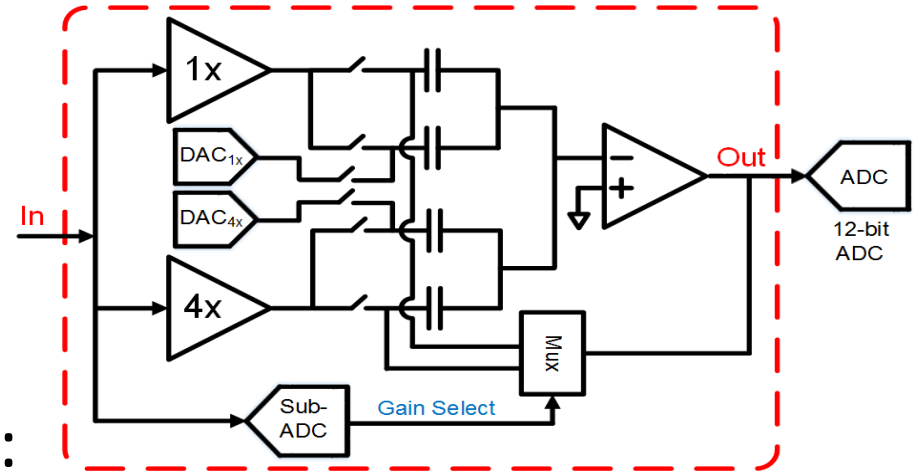


Reason for 34dB SFDR for 1.6V_{pp} diff input



- During PhiS cycle: All cap charge to input
- When PhiSadv is off (bottom plate sampling) Ideally no current should flow.
- Practically, current flows: Introduces distortion at output

Possible Solutions



1) Avoid bottom plate sampling:

- Problem: Charge injection when Sampling switch opens
- Rough calculations -> Expecting SFDR of 60dB: Not good enough

2) Make sure one branch is always off if sample taken from the other branch:

- Careful timing needed

- Results using 2nd approach: With verilogA logic:
  - Autoselect mode achieved 73dB SDR with ideal amplifier, switches and ideal 12 bit ADC.
- Next: work on transistor level schematics for autoselect

Next steps

- Need to design output buffers and run more tests.
- Schematic level work should be complete before March 20th
- Plan to complete layout by April 15th
- A bit tight schedule. Need exact gds submission date for better planning.
- Work division required for integrating DRE with 12-bit ADC.